
Chip Support Library

Release Notes

Applies to Product Release: 2.0.0.19
Publication Date: Mar 27, 2014

Document License

This work is licensed under the Creative Commons Attribution-NoDerivs 3.0 Unported License. To view a copy of this license, visit <http://creativecommons.org/licenses/by-nd/3.0/> or send a letter to Creative Commons, 171 Second Street, Suite 300, San Francisco, California, 94105, USA.

Contributors to this document

Copyright (C) 2012-2014 Texas Instruments Incorporated - <http://www.ti.com/>



Texas Instruments, Incorporated
20450 Century Boulevard
Germantown, MD 20874 USA

Contents

Overview	1
New and Updated Features	1
Resolved IRs	6
Known Issues / Limitations	6
Licensing.....	6
Delivery Package	6
Directory Structure	6
Installation Instructions.....	7
Instruction for RTSC getLibs	7
Customer Documentation List	7

Chip Support Library version 2.0.0.19

Overview

This release of CSL contains peripheral programming (functional and register level) APIs. The list of modules supported in this release is listed in later sections. This set of APIs provides peripheral abstraction that can be used by higher layers of software.

This is an initial alpha release to support early integration for TCI6634K2K, TCI6638K2K and TCI6636K2H KeyStone II devices.

This release includes:

- Compiled library of supported CSL modules for multiple KeyStone II devices
- Source
- API reference guide

New and Updated Features

Table 1 CSL Modules included in this Release

Peripherals	TCI6634K2K/TCI6638K2K/TCI6636K2H CSL-RL Available	Comments
AIF 2.1	X	
AT	X	
BCP	X	
BCR	X	
BOOTCFG	X	
CGEM	X	
CHIP	X	
CP_BOOTCFG	X	
CP_INTC 0..2	X	
CP_MPU	X	
CPPI	X	
DEVICE	X	

DDR3/EMIF4 DDR3a (64b) w DDR3a PLL DDR3b (64b) w DDR3b PLL	X	
EDMA	X	
EMAC (SGMII, CPSWITCH, MDIO)	X	
EMIF16	X	
FFTC A/B/C/D/E/F	X	
GPIO	X	
Hyperlink	X	
I2C	X	
IPC	X	
MSMC	X	
NetCP (PASS)	X	
PCIE	X	
PSC	X	
QMSS 1.5	X	
RAC v1.2 A/B/C/D	X	
SA	X	
SEC_MGR		
Smart Reflex 0		
Smart Reflex 1 (ARM)		
Semaphore	X	
SPI 0/1	X	
SPI 2	X	
SRIO	X	
TAC 2	X	
TCP3D A/B/C/D	X	
TIMER64P	X	
UART	X	
USIM	X	
USB	X	
VCP A/B/C/D/E/F/G/H	X	
Tetris	X	
TSIP (For TCI6608T)	X	
XGE (5 Port Switch)	X	

XMC	X	
-----	---	--

The following is the naming convention for the various CSL prebuilt library files:

Default Directory	Library Name	Description
ti\cs1\lib\k2k\c66	ti.csl.ae66	66 ELF Little Endian Library
ti\cs1\lib\k2k\c66	ti.csl.ae66e	66 ELF Big Endian Library
ti\cs1\lib\k2k\c66	ti.csl.intc.ae66	66 ELF Interrupt Controller Little Endian
ti\cs1\lib\k2k\c66	ti.csl.intc.ae66e	66 ELF Interrupt Controller Big Endian
ti\cs1\lib\k2h\c66	ti.csl.ae66	66 ELF Little Endian Library
ti\cs1\lib\k2h\c66	ti.csl.ae66e	66 ELF Big Endian Library
ti\cs1\lib\k2h\c66	ti.csl.intc.ae66	66 ELF Interrupt Controller Little Endian
ti\cs1\lib\k2h\c66	ti.csl.intc.ae66e	66 ELF Interrupt Controller Big Endian

Release 2.0.0.19 Updates:

- IR fixes see Resolved IRs

Release 2.0.0.18 Updates:

- IR fixes see Resolved IRs

Release 2.0.0.17 Updates:

- Following are the SERDES configuration updates available in this release:
 - SERDES configuration support for 10 Gig for 156.25Mhz and link rates 10.3125G and 1.25G
 - AIF2:

- API CSL_AIF2SerdesInit() being renamed to CSL_AIF2SerdesInitB8. No migration impact if AIF2 LLD is being used
- Additional API CSL_AIF2SerdesInitB4 available for B4 PLL
- Hyperlink
 - Additional support for 6Gig/10Gig/12.5G rate for reference clock config: 156.25Mhz and 312.5Mhz
- Ethernet, Hyperlink ,PCIE and SRIO:
 - Fix for CSL_XXXSerdesGetStatus for Lane OK status. Removed check for Signal Detect status as being not required during init time SERDES configuration

Release 2.0.0.16 Updates:

- Bug fixes. Refer Resolved IRs section.

Release 2.0.0.15 Updates:

- Bug fixes. Refer Resolved IRs section.
- Updated AIF2 SERDES CSL

Release 2.0.0.14 Updates:

- Add Qmss_QueueType_INTC_SET[234]_QUEUE to csl_qm_queue.h to support all of the INTC/CIC queues.

Release 2.0.0.14 Updates:

- Remove CSL_QMSS_DATA_QM#_QUEUE_PROXY_REGS which is an unsupported address in the HW.
- Add XGE to csl_cpqi.h

Release 2.0.0.13 Updates:

- Updated bootcfg CSLs for TCI6634K2K and TCI6636K2H (SDOCM00100201)
- Bug fixes. Refer Resolved IRs section.

Release 2.0.0.12 Updates:

- Updated queue assignments for K2K and K2H as per spec version 1.7.
- Updated cslr_pll.c.h for new register additions
- Added SERDES CSL-RL files
- Updated cslr_emif4f.h with register name corrections
- Re-arranged some CSL files to support multiple versions of an IP in the same package

Release 2.0.0.11 Updates:

- Updated device and interrupt CSL header files to 1.2 and 1.1 versions respectively.

Release 2.0.0.10 Updates:

- Updated AIF 2.1 CSL-RL and CSL-FL

Release 2.0.0.9 Updates:

- Updated `csl_device_interrupt.h` for name changes
- Added `#ifdef` around instance specific base register addresses in `CSL_XXXXGetBaseAddress()` functions.

Release 2.0.0.8 Updates:

- New directory naming conventions i.e. `k2k` represents TCI6634K2K and TCI6638K2K while `k2h` represents TCI6636K2H
- Addition of TCI6636K2H support

Release 2.0.0.7 Updates:

- Updates for using auto-generated `cslr_device.h` and `csl_device_interrupt.h` files.

Release 2.0.0.6 Updates:

- Added CSL-RLs for Tetris and USB
- Updated directory structure for Library location to top level `lib/<device>/c66` folder

Release 1.0.0.5 Updates:

- Added CSL-RLs for XGE (10 Gig Ethernet) IP
- Minor updates to EMAC (CPSW-5GF) and MDIO CSL-RLs
- Added support for remaining 4 VCP instances (E, F, G and H) in `csl_vcp2.c`

Release 1.0.0.4 Updates:

- Updated CSL queue assignment and CPDMA support
- Includes updated version of TCI6634 CSL device interrupt file
- Added `cslr_srio_resetread.c` for SRIO CSL-FL

Release 1.0.0.3 Updates:

- ARM support

Release 1.0.0.2 Updates:

- Added `csl_emif4fGetBaseAddress.c` to support multiple instances of DDR3
- Included `csl_tsipGetBaseAddress.c`
- Updated `csl_racGetBaseAddress.c` to use `RAC_A DATA_FEI_REGS` for `RAC_B`, `RAC_C` etc.

- Updated `cslr_device.h` for TSIP
- Updated `csl_device_interrupt.h` for tci6608t to align with the latest interrupt release
- Updated CSL-RLs for BCP, EMIF4, EMAC (CPSW-5GF), PA, SGMII, MDIO and Semaphore
- Added CSL-RL for USIM

Release 1.0.0.1000 Updates:

- Initial CSL Engineering Release supporting TCI6634 and TCI6608T devices

Resolved IRs

IR Parent/ Child Number	Severity Level	IR Description
SDOCM00106647	Major	Bug in CSL Serdes 10GE API
SDOCM00107192	Major	Updates to Serdes Config files for Hyperlink/SRIO

Known Issues / Limitations

The release has undergone limited testing on simulator. Current Known issues at the time of release includes:

IR Parent/ Child Number	Severity Level	IR Description

Licensing

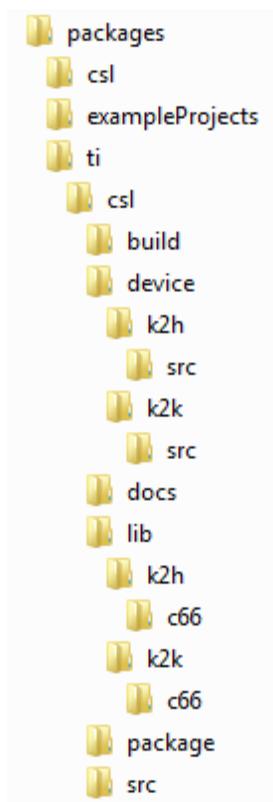
BSD Licensing

Delivery Package

Package is delivered as full source release in tar format.

Directory Structure

Following is the directory structure after CSL tar package is extracted.



Installation Instructions

Extract the tar package in a destination directory.

Instruction for RTSC getLibs

In order to retrieve CSL library for a device using getLibs following line would be required in RTSC configuration file.

```

/* Load and use the CSL package */
var Csl = xdc.loadPackage('ti.csl.device.k2k.c66');

```

Replace k2k with the appropriate device name for the library being included

Customer Documentation List

Table 1 lists the documents that are accessible through the **/docs** folder on the product installation CD or in the delivery package.

Table 1 Product Documentation included with this Release

Document #	Document Title	File Name
1	API documentation (generated by Doxygen)	csl/docs/csldocs.chm